What is claimed is:

1. An electronic device supported on a semiconductor substrate comprising:

a diffusion area in said substrate and a polysilicon area comprising a polysilicon layer extending over said substrate for contacting said diffusion area; and

a single contact disposed on top of said substrate contacting both said polysilicon layer and said diffusion area.

2. The electronic device of claim 1 further comprising:

a field oxide disposed next to said diffusion area wherein said polysilicon layer disposed on top of said field oxide and extending therefrom to contact said diffusion area.

3. The electronic device of claim 1 further comprising:

a metal layer disposed on top of said single contact for connecting to another circuit element of said electronic device.

4. The electronic device of claim 1 wherein:

said single contact further comprising a conductive material filling a contact opening etched in an insulating layer overlying said diffusion area and said polysilicon area.

5. The electronic device of claim 1 wherein:

said electronic device further comprising a transistor and said diffusion area further comprising a source/drain of said transistor.

6. A ploy-to diffusion connection (PDC) disposed on a substrate comprising:

a diffusion area in said substrate and a polysilicon area comprising a polysilicon layer extending over said substrate for contacting said diffusion area.

7. The PDC of claim 6 further comprising:

a single contact disposed on top of said substrate contacting both said polysilicon layer and said diffusion area.

8. The PDC of claim 6 further comprising:

a field oxide disposed on said substrate next to said diffusion area wherein said polysilicon layer disposed on top of said field oxide and extending therefrom to contact said diffusion area.

9. The PDC of claim 7 wherein:

said single contact further comprising a conductive material filling a contact opening etched in an insulating layer overlying said diffusion area and said polysilicon area.

10. The PDC of claim 7 further comprising:

a metal layer disposed on top of said single contact for connecting to another circuit element disposed on said substrate.

11. A method for configuring an electronic device on a semiconductor substrate comprising:

forming a diffusion area in said substrate;

configuring a polysilicon area by forming a polysilicon layer extending over said substrate for contacting said diffusion area; and

forming a single contact on top of said substrate contacting both said polysilicon layer and said diffusion area.

12. The method of claim 11 further comprising:

forming a field oxide next to said diffusion area and forming said polysilicon layer on top of said field oxide and extending therefrom to contact said diffusion area.

13. The method of claim 11 further comprising:

forming a metal layer on top of said single contact for connecting to another circuit element of said electronic device.

14. The method of claim 1 wherein said step of forming said single contact further comprising:

etching a contact opening in an insulating layer that overlying said diffusion area and said polysilicon layer; and

filling said contact opening with a conductive material.

15. The method of claim 11 wherein:

said method of configuring said electronic device further comprising a step of forming a transistor by employing said diffusion area as a source/drain of said transistor.

16. A method for forming a ploy-to diffusion connection (PDC) on a substrate comprising:

forming a diffusion area in said substrate and forming a polysilicon area by extending a polysilicon layer from said polysilicon area over said substrate to said diffusion area for contacting said diffusion area.

17. The method of claim 16 further comprising:

forming a single contact on top of said substrate contacting both said polysilicon layer and said diffusion area.

18. The method of claim 16 further comprising:

forming a field oxide on said substrate next to said diffusion area and forming said polysilicon layer on top of said field oxide and extending therefrom to contact said diffusion area.

19. The method of claim 17 wherein said step of forming said single contact further comprising:

etching a contact opening in an insulting layer overlying said diffusion area and said polysilicon area; and

filling said contact opening with a conductive material.

20. The method of claim 17 further comprising:

forming a metal layer on top of said single contact for connecting to another circuit element disposed on said substrate.